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ELECTROMAGNETIC PLATFORM FOR LIGHTWEIGHT INTEGRATION/INSTALLATION OF ELECTRICAL SYSTEMS IN COMPOSITE ELECTRICAL AIRCRAFT

HIGH-LEVEL MODELING OF COSMIC RADIATION EFFECTS

OFFICE NATIONAL D'ETUDES ET DE RECHERCHES AEROSPATIALES (ONERA)

Toulouse, France

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https://ec.europa.eu/programmes/horizon2020 http://caric.aero http://www.nserc-crsng.gc.ca

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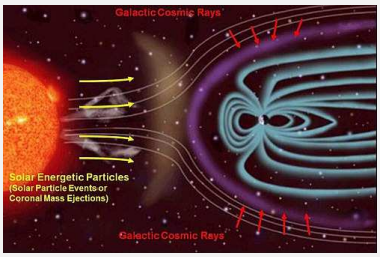
AGENDA

1. Introduction
2. Objectives
3. Target avionics systems
4. Proposed approach
5. Results
6. Conclusion

1. INTRODUCTION

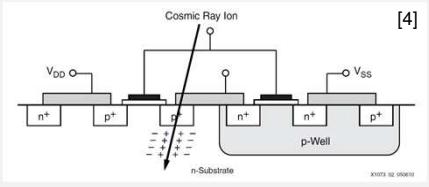
- Cosmic radiation (CR): high energy particles (protons, heavy ions, etc.)
- Sources of CR [1]:
  - Galactic cosmic rays
  - Solar flares
- Good (but not perfect) protection from Earth magnetic field + atmosphere
- For avionics systems, primarily concern : neutrons [1]



Source: [2]

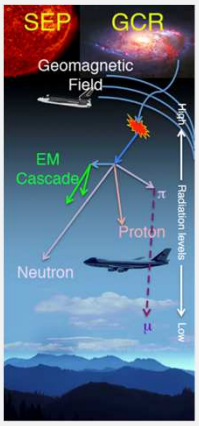
1. INTRODUCTION

- Impact of a high-energy neutron on silicon substrate [4]:
  - Charged particles created by collisions
  - If enough charge, state of a static memory element can be changed: SEUs.



2. OBJECTIVES

- Questions:
  - How sensitive to CR avionics systems really are?
  - How do avionics systems react to SEUs induced by CR?
    - How to model SEUs impact on avionics systems early in the design process?



[2]

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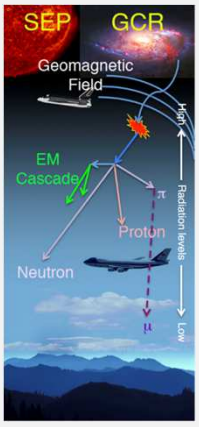
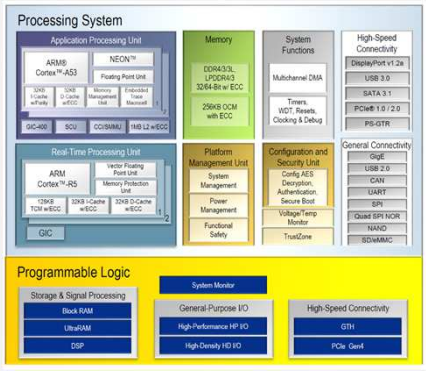


[2]

3. TARGET AVIONICS SYSTEMS

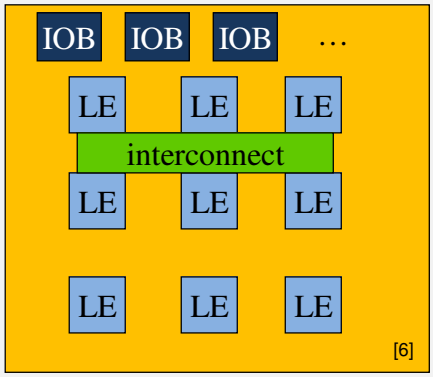
- SRAM FPGA-based avionics systems
  - SRAM-based FPGAs
    - Increasingly popular for avionics and space applications
      - State-of-the-art technology
        - High density
        - High frequency
        - Reasonable power
      - Fast time to market
      - Easily (re)programmable



Zynq® UltraScale+™ MPSoCs [5]

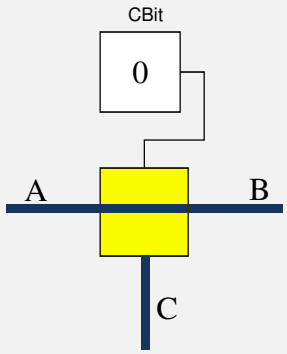
3. TARGET AVIONICS SYSTEMS

- SRAM-based FPGAs
  - Reprogrammability from SRAM configuration bits:
    - Define logic functions
    - Define routing to connect used resources



3. TARGET AVIONICS SYSTEMS

- SRAM-based FPGAs
  - Drawback:
    - Sensitive to CR
      - Configuration bit state modified
      - Corrupted logic functions or routing



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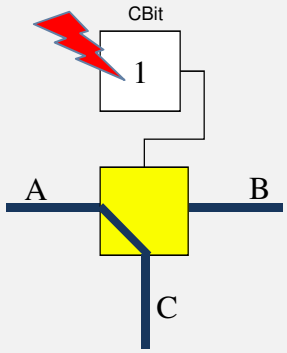
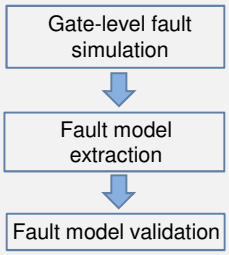


4. PROPOSED APPROACH

- How to model SEUs impact on SRAM FPGA-based avionics systems early in the design process?
- High-level simulation
  - High-level fault injection, to be used early in the design process
  - Allowing designers to know how their systems will behave when affected by SEUs caused by CR
  - Target: Matlab/Simulink
  - Need high-level fault models



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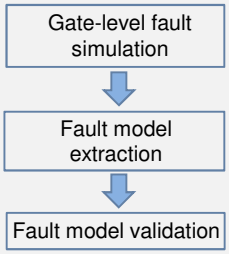
- Target gate-level fault model
  - Stuck-at fault
    - Simple
      - s@0: node stuck at logical value 0
      - s@1: node stuck at logical value 1
    - Widely used in IC test
    - Existing tools
    - Fits well with CR impact



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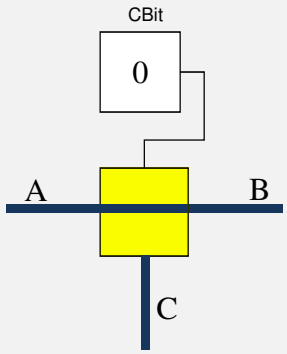

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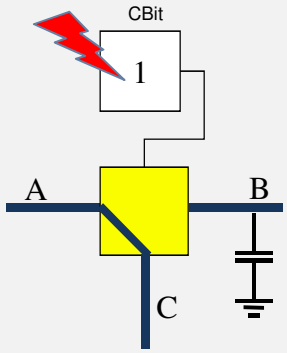
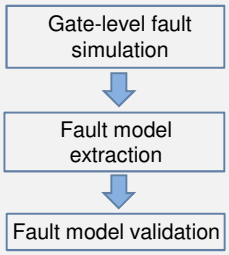


Node stuck at the value it had before the SEU

4. PROPOSED APPROACH

- Proposed high-level fault models
  - Simple
  - Applied only on block I/Os
    - Avoid modifying Matlab/Simulink blocks
    - Help reducing the number of injected faults
  - Hopefully cover most of the cases



5. RESULTS

- First target circuits
  - Combinational: adder + multiplier
  - Extracted high-level models:
    - Stuck-at faults on the I/Os
  - Validation:
    - Using bombardment results from TRIUMF
      - Xilinx Virtex-5 FPGA
      - Proton beam, 105MeV

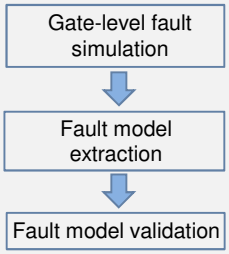


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Table 1: TRIUMF results from 16-bit adder

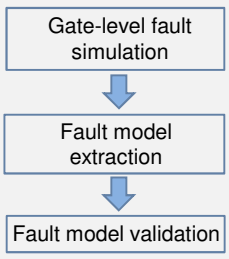
Faulty cases	Faulty cases with stuck-at behaviour on I/Os	Coverage offered by I/O stuck-at (%)
43841	43835	99.99

Table 2: TRIUMF results from 8x8 multiplier

Faulty cases	Faulty cases with stuck-at behaviour on I/Os	Coverage offered by I/O stuck-at (%)
24435	24409	99.89

5. RESULTS

- Second target circuits
  - Sequential: B01, B05, B12 from ITC99 benchmark
  - Extracted high-level models:
    - Stuck-at on the I/Os
    - Additional circuit (registers + mux) in case clock and reset signals not available in Matlab/Simulink block models
  - Validation:
    - Using SEM emulation
      - Xilinx Artix-7 FPGA



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Item	B01	B05	B12
PIs	2	1	5
POs	2x1	5x7,1x1	2x1,1x4
Gates	46	935	1036
FFs	5	34	121
Setup	1440	108	72

5. RESULTS

- SEM emulation validation results:
  - We compare:
    - Faulty sequences obtained with SEM emulation
    - Faulty sequences with stuck-fault on I/Os obtained with gate-level fault simulation (GLFS); the one matching the most each SEM faulty case
  - Sequences of outputs obtained with 2047 pseudo-random test patterns after SEU detection
  - Goal: to have high-level fault models producing sequences of outputs that are at least as faulty as the ones from emulation
  - Coverage definition, for each sequence
    - $\sum NFS(GLFS,k) \geq \sum NFS(SEM,k)$, **OVERALL**
  - Coverage definitions, for each test pattern *k*:
    - $NFS(GLFS,k) \geq NFS(SEM,k)$, **At least as faulty (ALAF)**
    - $0 < NFS(GLFS,k) < NFS(SEM,k)$, **PARTIAL**
    - $0 = NFS(GLFS,k),\ 0 < NFS(SEM,k)$, **NO**

Item	B01	B05	B12
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- NFS() = Number of faulty signals (bus or bit)

Patterns	GLFS		SEM		NFS		coverage	
	A	B	A	B	GLFS	SEM	type	%
k=1					2	2		
k=2					2	0	ALAF	60
k=3					1	1		
k=4					1	2	PARTIAL	20
k=5					0	1	NO	20
ALL					6	6	OVERALL	100

- Coverage definitions, for each test pattern *k*:
  - NFS(GLFS,k) ≥ NFS(SEM,k), **At least as faulty (ALAF)**
  - 0 < NFS(GLFS,k) < NFS(SEM,k), **PARTIAL**
  - 0 = NFS(GLFS,k), 0 < NFS(SEM,k), **NO**

- NFS() = Number of faulty signals (bus or bit)

5. RESULTS

Coverage (%)	B01		B05		B12	
	Alone	At least	Alone	At least	Alone	At least
ALAF	95.5	95.5	98.6	98.6	100	100
PARTIAL	2.2	97.7	0.1	98.6	0.0	100
NO	2.3	100	1.3	100	0.0	100
OVERALL	100		100		100	

producing sequences of outputs that are at least as faulty as the ones from emulation

- Coverage definition, for each sequence
  - ∑NFS(GLFS,k) ≥ ∑NFS(SEM,k), **OVERALL**
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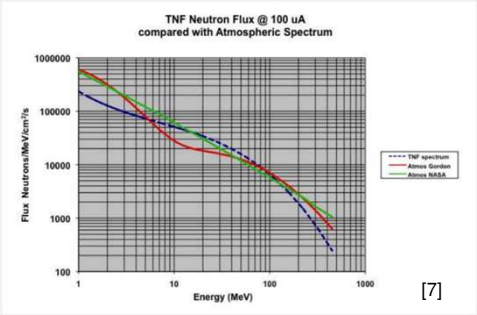
5. RESULTS

- Status for validation using bombardment results from TRIUMF
  - Experiments completed, May 23-24
  - Neutron beam



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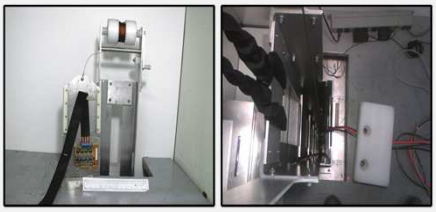

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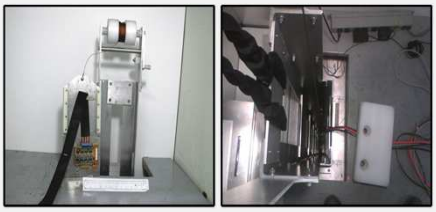
  - **ANALYSIS DONE!**



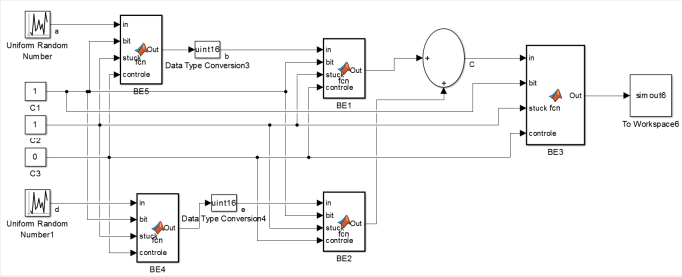
5. RESULTS

Coverage (%)	B01		B05		B12	
	Alone	At least	Alone	At least	Alone	At least
ALAF	95.0	95.0	98.8	98.8	100	100
PARTIAL	2.9	97.8	1.1	99.9	0.0	100
NO	2.2	100	0.1	100	0.0	100
OVERALL	100		100		100	
Faulty seq.	80		66		52	

- **ANALYSIS DONE!**

5. RESULTS

- Modeling in Matlab/Simulink:
  - Done for combinatorial circuits + B01 (sequential)



6. CONCLUSION

- We proposed and developed high-level fault models allowing fault injection early in the design process
- Target: Matlab/Simulink
- Usable in other environments/levels (gate-level, register transfer level, …)
- Based on the widely applied stuck-at fault model
- Fully validated for combinational circuits
- Fully validated for sequential circuits
- These models will allow designers to know, early in the design process, how their systems will react to SEUs caused by CR

REFERENCES

[1] E. Petersen, “Single Event Effects in Aerospace,” Wiley, 2011.

[2] Wikipedia

[3] E. Normand, “Single Event Effects in Avionics,” IEEE Trans. On Nuclear Science, vol. 43, no. 2, April 1966, pp. 461-474

[4] C. Hu and S. Zain, “NSEU Mitigation in Avionics Applications ,” Xilinx App. Note XAPP1073 (v1.0) May 17, 2010.

[5] Xilinx, “Zynq® UltraScale+ MPSoC Product Tables and Selection Guide”, XMP104 (v2.1), www.xilinx.com

[6] W. Wolf, FPGA-Based System, Prentice Hall, 2004.

[7] www.triumf.ca

[8] N. Weste and D. Harris, *CMOS VLSI Design: A Circuits and Systems Perspective*, 4th Edition, Addison Wesley, Reading (Mass.), 2011.

THANK YOU FOR YOUR ATTENTION! ANY QUESTION?

THANK YOU

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